Remarks/Arguments

Claims 1-12 are pending. Claims 1, 2, 5-7, 9, 11 and 12 have been rejected. Claims 3-4, 8 and 10 are indicated to be allowable over the cited prior art.

Responsive to the comments regarding the specification, Applicants have amended the specification to include headings as necessary. No new matter has been added.

Rejection of claims 1, 2 and 5 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,745,468 issued to Nakano (hereinafter, "Nakano")

Applicants submit that Nakano fails to teach each and every limitation recited in independent claim 1, and as such, claims 1, 2 and 5 are not anticipated under 35 U.S.C. §102(b) by Nakano.

Independent claim 1 recites:

> *a first clock generator for generating a reference clock signal, the* ***reference clock signal being independent of the synchronizing characteristic of the analog signal;***
> *a second clock generator, coupled to the first clock generator, for producing a plurality of further clock signals in response to the reference clock signal ...*
> *the* ***A/D converters being clocked by respective ones of the plurality of further clock signals, which are independent of the synchronizing characteristic of the input analog signal*** *and have a frequency substantially equal to the sampling rate, whereby corruption of the analog signal by digital noise in the apparatus is prevented. (emphasis added)*

The Office Action alleges that Nakano teaches a first reference clock generator arrangement (22, 23) that is **independent of the input signal**, a second reference clock generator arrangement that is a function of the first clock generator arrangement (24, 25), and plural A/D convertors 5 and 6 that are coupled and responsive to the second clock generator arrangement, in which the second clock is **independent of the input signal**. Particularly, the Examiner contends that the system of Nakano as shown in Fig. 6 teaches a first reference clock generator (22, 23) that is 'based on the disk medium' and is independent of the input signal (see Office Action, page 3).

Applicants respectfully disagree that Nakano teaches a first reference clock generator that is independent of the input signal. In column 5, lines 1-7, Nakano states:

> *... a clock G (LCLK) synchronized with a leading or rising edge of this binary signal DRF is generated by the PLL circuit 3 as illustrated in FIG. 2. On the other hand, another* ***clock I (TCLK) synchronized with a trailing or falling edge of the signal DRF*** *is generated by the PLL circuit 4 as shown in FIG. 2. These clocks are supplied to the A/D converters 5 and 6, respectively. (emphasis added)*

As shown in Fig. 6, clock G is applied to A/D converter 5 and clock I is applied to A/D converter 6.

Clearly, Nakano is using a characteristic (leading and trailing edges) of the reproduction signal, coded as clock pits on the disc medium, to generate and adjust the clock signals LCLK and TCLK. Thus, Nakano is using a characteristic of the input signal to generate a reference clock signal contrary to the limitation of claim 1 which provides for the generation of a reference clock signal that is independent of the synchronization characteristic of the input signal. Nakano's reference clock signal generation is dependent on a characteristic of the reproduction (input) signal (i.e. clock pits on the disk medium) even if the clock pits are encoded onto the disk medium separately from the reproduction signal.

Further, Nakano teaches that the A/D converters are clocked by LCLK and TCLK, which are generated in response to a characteristic of the input signal. Specifically, Nakano states:

> *The A/D converters 5 and 6 perform the sampling of the reproduction signal RF having the waveform E of FIG. 2 according to the clocks supplied thereto.* ***The timing of the sampling is determined according to the clock LCLK or TCLK as being in synchronization with the leading edge or the trailing edge of the reproduction signal.*** *Further, it is assumed that as a result of sampling the signal RF by the A/D converter 5 in synchronization with the clock LCLK, pulses D10 to D19 (see H of FIG. 2) are obtained, and that as a result of sampling the signal RF by the A/D converter 6 in synchronization with the clock TCLK, pulses D20 to D29 (see J of FIG. 2) are obtained. Practically, the A/D conversions are performed in the A/D converters 5 and 6 by using data consisting of 6 to 8 bits. (emphasis added)*

By contrast, present claim 1 recites, "... A/D converters being clocked by respective ones of the plurality of further clock signals, which are independent of the synchronizing characteristic of the input analog signal and have a frequency substantially equal to the

sampling rate, whereby corruption of the analog signal by digital noise in the apparatus is prevented." Therefore, applicants submit that Nakano also fails to disclose or suggest this limitation of claim 1.

In view of the above, Applicants submit that Nakano fails to disclose or suggest each and every the limitations of independent claim 1, and as such, Nakano does not anticipate independent claim 1, or claims 2 and 5, which depend therefrom. Withdrawal of the rejection to claims 1, 2 and 5 is thus respectfully requested.

Rejection of claims 6, 7, 9, 11 and 12 under 35 USC §103(a) as being unpatentable over Nakano and further in view of U.S. Patent 4,138,741 issued to Hedlund et al. (hereinafter, "Hedlund")

Applicants submit that for the reasons discussed below, claims 6, 7, 9, 11 and 12 are patentably distinguishable over the teachings of Nakano and Hedlund.

Independent claims 6 and 9 both recite a first clock generating circuit for generating a reference clock signal that is independent of an input signal, and A/D converters that are clocked by clock signals that are independent of the synchronizing characteristic of the input signal, in a manner similar to independent claim 1. For the reasons discussed above, applicants submit that Nakano also fails to disclose or suggest at least these limitations as applied to claims 6 and 9.

Hedlund is cited as allegedly teaching specific signal types that may be processed in a disk storage system since Nakano does not specify the signal type being processed. However, assuming arguendo that Hedlund teaches this feature, Hedlund still fails to cure the above-mentioned defect of Nakano as applied to claims 6 and 9.

Since Hedlund fails to overcome the defect of Nakano as applied to claims 6 and 9, Applicants submit that claims 6 and 9, and claims 7, 11 and 12, which depend therefrom, are patentably distinguishable over the combination of Nakano and Hedlund. Withdrawal of the rejection of claims 6, 7, 9, 11 and 12 is thus respectfully requested.

Having fully addressed the Examiner's objections and rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, entry of this amendment, reconsideration of the claims, withdrawal of the objections and rejections thereto, and allowance of all claims are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6815, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed to be incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832.

Respectfully submitted,
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I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia, 22313-1450 on:

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